Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 52458

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017

Sixth Semester

Electronics and Communication Engineering

EC 2354 – VLSI DESIGN

(Common to Biomedical Engineering)

(Regulations 2008)

(Also Common to PTEC 2354 – VLSI Design for B.E. (Part-Time) Fifth Semester-Electronics and Communication – Regulations 2008)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. What is meant by subthreshold voltage ?
2. What is design for manufacturability ?
3. Define energy delay product.
4. Write the benefits of scaling.
5. What is meant by bubble pushing ?
6. Define clock skew.
7. List the various levels in testing of die.
8. What is the need of shmoo plots ?
9. Find the logic effort for four input NAND gate ?
10. What is DUT ?

PART – B (5×16=80 Marks)

11. a) Explain the various operation region of MOS transistor with its characteristics. (16)

(OR)

b) Discuss the CMOS process flow with neat diagram. (16)

12. a) i) Illustrate the interconnect and its effects in IC design. (10)

ii) Explain the types of power dissipation. (6)

(OR)

b) Explain the device characterization and circuit characterization. (16)

13. a) i) Explain the operation of master slave edge triggered register. (8)

ii) Discuss the signal integrity in dynamic design. (8)

(OR)

b) Briefly discuss about the synchronizer in digital design. (16)

14. a) Illustrate the design procedure to test chip after fabrication. (16)

(OR)

b) Discuss the main approaches in DFT with suitable example. (16)

15. a) Write VHDL coding for the priority Encoder and full adder. (16)

(OR)

b) Write VHDL coding for the 3 × 8 decoder using behavioral model and data flow model. (16)